Three Dimensional CFD Simulations of Junction Temperature of Electronic Components Using Nano-Silver

Mazlan Mohamed[1] and Rahim Atan[2]

[1]Faculty of Mechanical Engineering, Universiti Teknologi MARA,
Pulau Pinang Campus, 13500 Permatang Pauh, Pulau Pinang, Malaysia
[2]Faculty of Mechanical Engineering, Universiti Teknologi MARA,
40450 Shah Alam, Selangor, Malaysia
[1]Email: mazlan547@ppinang.uitm.my

ABSTRACT

This paper presents the simulation of three dimensional numerical analyses of heat and fluid flow through chip package. 3D model of chip packages is built using GAMBIT and simulated using FLUENT software. The study was made for four chip packages arranged in line under different types of materials, inlet velocities and package (chip) powers. The results are presented in terms of average junction temperature and thermal resistance of each package The comparison between three types of material in terms of junction temperature has been observed and it was found that the junction temperature of the nano-silver had the lowest junction temperature as compared to epoxy and composite polymer. It also found that the nano-silver had the highest value of thermal conductivity as compared to the others. The strength of CFD software in handling heat transfer problems is proved to be excellent.

Keywords: *PLCC package, Thermal conductivity, Numerical simulation, Average junction temperature, Nano-Silver*

INTRODUCTION

Nowadays, the major trend in electronic industry is to make the products smarter, lighter, functional and highly compact. At the same time the

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products can reduce the heat of electronic component. This trend has necessitated stringent packaging requirements and using nanotechnology is a promising option to tackle this issue. However, a serious issue in electronic packaging is the thermal management. The electronic components made using silicon chip and the organic substrate generates heat and causes malfunction for some electronic components when the temperature above 70 ºC. This problem is effectively solved by using nano-Silver in chip packaging because it can dissipate heat more effectively. Moreover, it protects the chip from moisture, ionic contaminants, radiation, thermal expansion and vibration. Conventionally the chip packages were made by epoxy or silicon as main material in the electronic components in chip manufacturing. In this case, when electronic components operate in long period, the temperature of chip in electronic components will easily exceed 70 ºC. This will cause electronic components malfunction or overheated. That why there are a lot of researchers doing study on thermal management over 30 years ago.

Nanotechnology has nowadays become a very important part in developing advanced electronic industries. In electronic industries, the continuing increase of power densities in microelectronics and simultaneous drive to reduce the size and weight of electronic products have led to the increased importance of thermal management issues in electronic industry. The temperature at the junction of an electronic package has become an important factor that determines the lifetime of the package. The thermal management has started since 30 years ago. Initially, the studies have been conducted by experiment only. The heat transfer and pressure drop for airflow in arrays of heat generating rectangular module was studied by Sparrow in 1982 [1]. Later Sparrow (1983) [2] made an experimental investigation of heat transfer and fluid flow characteristics of arrays of heat-generating block-like modules affixed to one wall of a parallel-plate channel and cooled by forced convection airflow. He also investigated the convective heat transfer response to height differences in an array of block-like electronic components. Gupta and Jaluria [3] carried out experiments to study forced convection water cooling of arrays of protruding heat sources with specified heat input. Hwang [4] investigated forced convection from discrete heat sources mounted flush on a conductive substrate in a rectangular duct. Molki and Faghri [5] made an experimental investigation of forced convection air-cooling of a 4-by-3 copper rectangular block

positioned along the lower wall of the test section in an in-line arrangement. Ramadhyani, Moffat and Incropera [6] made a 2D numerical study on the conjugate analysis of forced convection heat transfer from discrete heat sources mounted on a solid substrate and exposed to fully developed laminar flow. Davalath and Bayazitoglu [7] considered a conjugate heat transfer for two-dimensional, developed flow over array rectangular blocks representing finite heat sources on parallel plate using the cooling fluid as air.

Utilization of CFD as thermal prediction tool was employed by Plotnik and Anderson [8] and Tucker and Paul [9] as part of design for heat transfer enhancement in electronic devices. The laminar and the turbulent forced convective flows over two sequentially heated blocks mounted on one principal wall of a channel were experimentally and numerically studied by Chen and Wang [10]. Hong and Yuan [11] proved that a constant and uniform heat transfer coefficient across the whole package was inadequate in the accurate prediction of thermal stresses, due to the significant effect of local temperature distribution resulted from the variation of local heat transfer coefficient. Thus, they demonstrated the importance of considering the conjugate problem for electronic packages. Jayakanthan et al. [12] carried out simulations of conjugate heat transfer associated with single and two packages mounted on printed circuit board (PCB) which was situated in a wind tunnel, using FLUENT™ for various flow conditions. This work was numerical investigation of heat transfer in plastic leaded chip carrier continued by Huat (1998) [13] who simulated multiple chips using a 2D model. Hung and Fu [14] designed a two-dimensional model for numerical prediction of viscous laminar flow, mixed convection and conjugated heat transfer between parallel plates with uniform block heat source and with opening on the integrated circuit board. The interest in the determination of junction temperature and thermal resistance continued to grow as is evident from the works of Tso et al. [15], Young and Vafai [16], and Kim and Kim [17].

In 2007, the development of electronic industries increase rapidly because of the development of nanotechnology. Nano-silver is used in electronic components to decrease temperature and increase the performance of chip processor. Nano-silver can decrease the junction temperature of chip compared with others material like epoxy compound moulding (EMC) and Composite polymer. As the modern electronic industry is driving

towards more compact systems, further research is needed to increase the performance of electronic devices. Accordingly, the present study is focused on simulations of PLCC packages by using new material, nano-silver as compared to the traditional one using epoxy moulding compound (EMC) and Composite polymer by using several inlet air velocities under natural, mixed and forced convection conditions with different chip powers. Factors affecting the chip temperature such as coolant velocity, chip power and thermal conductivity of materials are studied and presented.

THE NUMERICAL MODEL

Governing Equations

The basic equations describing the flow of fluid are conservation of mass, conservation of momentum and conservation of energy. The governing equations are expressed as:

Continuity equation:

$$\frac{\delta u}{\delta x}+\frac{\delta v}{\delta y}+\frac{\delta w}{\delta z}=0$$

Dimensionless continuity equation:

$$\frac{\partial \hat{U}}{\partial X}+\frac{\partial \hat{V}}{\partial Y}+\frac{\partial \hat{W}}{\partial Z}=0$$

Momentum equation:

x-direction

$$\left(u\frac{\delta u}{\delta x}+v\frac{\delta u}{\delta y}+w\frac{\delta u}{\delta z}\right)(\rho)=-\frac{\delta p}{\delta x}+\mu\left(\frac{\delta^2 u}{\delta x^2}+\frac{\delta^2 u}{\delta y^2}+\frac{\delta^2 u}{\delta z^2}\right)$$

y-direction

$$\left(u\frac{\delta v}{\delta x}+v\frac{\delta v}{\delta y}+w\frac{\delta v}{\delta z}\right)(\rho)=-\frac{\delta p}{\delta y}+\mu\left(\frac{\delta^2 v}{\delta x^2}+\frac{\delta^2 v}{\delta y^2}+\frac{\delta^2 v}{\delta z^2}\right)$$

z-direction

$$\left(u\frac{\delta w}{\delta x}+v\frac{\delta w}{\delta y}+w\frac{\delta w}{\delta z}\right)(\rho)=-\frac{\delta p}{\delta y}+\mu\left(\frac{\delta^2 w}{\delta x^2}+\frac{\delta^2 w}{\delta y^2}+\frac{\delta^2 w}{\delta z^2}\right)$$

Energy equation:

Energy balance equation with negligible radiation and distribute energy source in the fluid field is given as:

$$\rho c_p\left(u\frac{\delta T}{\delta x}+v\frac{\delta T}{\delta y}+w\frac{\delta T}{\delta w}\right)=k\nabla^2 T$$

Description of Model

The model used in this simulation consists of a wind tunnel which encompasses the whole computational domain with a motherboard and 4 PLCC made by nano-silver, epoxy moulding compound (EMC) and composite polymer. The isometric view, plan view, and front view of the simulation setup for 4 PLCC packages are shown in Figure 1. The motherboard (PCB) is set up 9 cm from the inlet of wind tunnel to make sure that the flow is fully developed when it reaches the outlet of the wind tunnel. The 4 PLCC packages, each having 2 cm $\times$ 2 cm face were mounted with 3 cm gaps on the PCB in a symmetrical manner as shown in Table 1. The setup is kept at a height of 7 cm from the bottom surface of the wind tunnel. The motherboard thickness is 0.015 cm and the thickness of chips is 0.3 cm each, both made from nano-silver and compared with PLCC made from epoxy moulding compound and composite polymer.

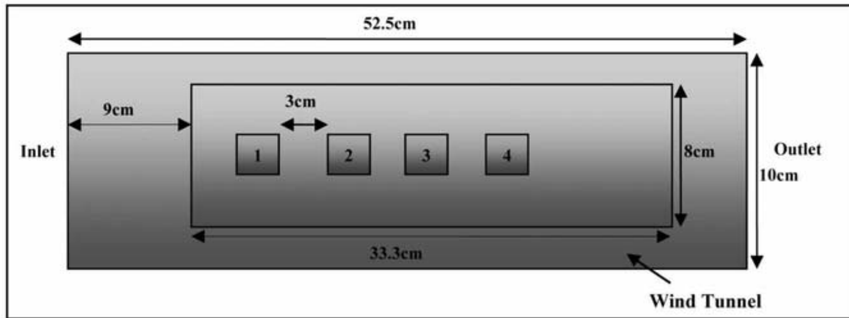


Figure 1: Simulation Setup for 4 PLCC Packages

Table 1: Dimension of Components Used in Simulation

Component	Quantity	Size (cm^3)
Wind tunnel	1	52.5 cm × 10 cm × 10 cm
Motherboard	1	33.3 cm × 0.15 cm × 8 cm
Chip	4	2 cm × 0.3 cm × 2 cm

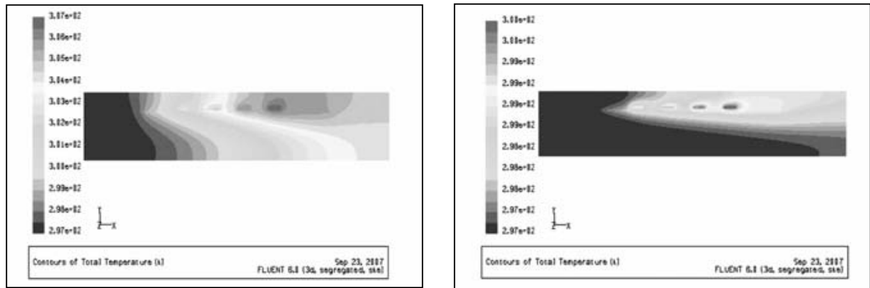
RESULTS AND DISCUSSION

The results are presented in terms of average junction temperature and thermal resistance for the packages under different operating conditions. The results of nano-silver are comparable with epoxy moulding compound and composite polymer where 3-D analysis of the heat and fluid flow are similar and having same model dimensions. The difference is he used only epoxy while this research used nano-silver material to optimize and to decrease junction temperature for each PLCC packages with different values of input velocity. The natural convection falls in the range of 0.001 m/s to 0.01 m/s, mixed convection from 0.01m/s to 0.1 m/s and forced convection from 0.1m/s to 2 m/s.

DIFFERENCES BETWEEN NANO-SILVER, EPOXY MOULDING COMPOUND AND COMPOSITE POLYMER ON AVERAGE JUNCTION TEMPERATURE

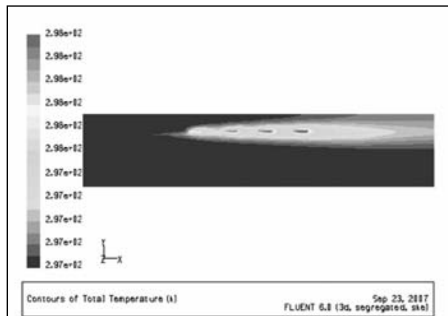
Chip Power 0.5 W

Figure 2 shows the comparison between epoxy and nano-silver in contour of total temperature for 4 PLCC at 1 W for velocities 0. 1 m/s.



a) 0.1 m/s, 0.5 W, 4 PLCC (Epoxy)

b) 0.1 m/s, 0.5 W, 4 PLCC (Composite Polymer)



c) 0.1 m/s, 0.5 W, 4 PLCC (Nano-Silver)

Figure 2: The Comparison Between Epoxy, Composite Polymer and Nano-silver in Contour of Total Temperature for 4 PLCC at 0.5 W for Velocities 0.1 m/s

Table 2: Junction Temperature for Epoxy, Composite Polymer and Nano-silver Material in PLCC Packages

	Average Junction temperature (Kelvin)		
Inlet air velocity (m/s)	Epoxy	Composite polymer	Nano-silver
0.01	312.2	309.4	306.6
0.1	306.5	303.1	299.7
1.0	299.4	297.3	292.4

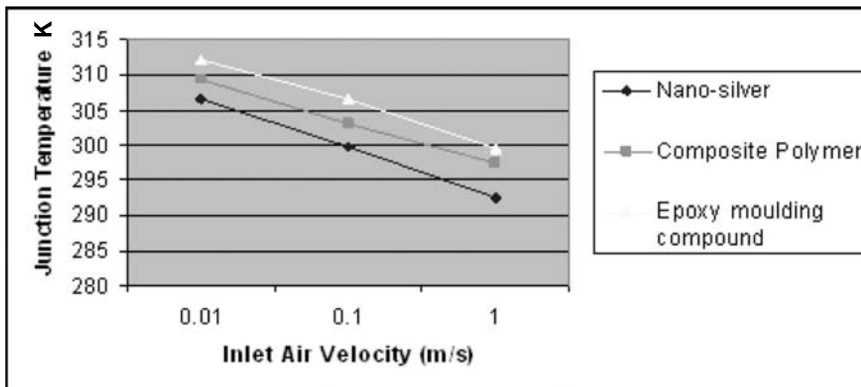


Figure 3: The Graph of Comparison Between Various Materials in Contour of Total Temperature for 4 PLCC at 0.5W for Velocities 0.01 to 0.1 m/s

The above results show that the junction temperature of each chip decreases with increase in inlet velocity, at a constant chip power. The junction temperature for nano-silver is lower than epoxy moulding compound (EMC) and Composite Polymer for air inlet veloctity at 0.01 m/s and 0.1.. The junction temperature of PLCC is reduced from 10-20 % by using nano-silver as compared to other materials. This happens due to the characteristic of nano-silver that has good thermal absorption and thermal resistance. The junction temperature for PLCC 1 is the lowest compared to the other packages whereas PLCC 4 has highest junction temperature. This phenomenon happens due to the flow resistance offered as the air passes over successive PLCC packages. In the simulation model, the arrangement of the packages begins with the PLCC 1 located in front of motherboard

followed by 2, 3 and 4. This makes the inlet air velocity to be minimum for PLCC 4 and hence maximum for junction temperature.

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